Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor, the method comprising:
depositing oxide fill on the n-type transistor and the p-type transistor and chemical/mechanical polishing the deposited oxide fill such that a gate stack of the n-type transistor and a gate stack of the p-type transistor, the n-type transistor and the p-type transistor each having spacers are surrounded with oxide,
etching a portion of the polysilicon from a gate of the p-type transistor;
depositing a low-resistance material on the p-type transistor and the n-type transistor; and
heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon of the p-type transistor and the polysilicon of the n-type transistor, such that compressive mechanical stresses are formed along a longitudinal direction of a channel of the p-type transistor.

[c2] The method of claim 1, further comprising removing a

portion of the deposited low resistance material.

[c3] The method of claim 1, further comprising:
covering an n-type transistor with a mask prior to performing the step of etching; and
removing the mask after performing the step of etching.

[c4] The method of claim 3, wherein the mask is a patterned photoresist layer.

[c5] The method of claim 1, wherein the step of depositing comprises depositing at least one of Co, HF, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr on the p-type transistor and then n-type transistor.

[c6] The method of claim 2, wherein the step of removing comprises removing a portion of the deposited low-resistance material with a selective etching technique.

[c7] The method of claim 1, wherein the step of heating comprises heating the integrated circuit to a temperature of about 300°C to about 1000°C.

[c8] The method of claim 1, wherein the step of depositing a low-resistance material comprises depositing a low-resistance material to a height of approximately 30Å-200 Å.

[c9] The method of claim 1, wherein the step of etching a

portion of the polysilicon comprises etching about half of the polysilicon from the p-type transistor.

[c10] The method of claim 1, wherein the step of etching comprises etching the polysilicon from the gate of the p-type transistor such that a n-type polysilicon to p-type polysilicon ratio is about 2:1.

[c11] The method of claim, wherein the etching comprises etching about 250 to about 750Å of the p-type polysilicon.

[c12] The method of claim 1, wherein the step of etching comprises etching the polysilicon from the gate of the p-type transistor using a wet etch or a dry etch.

[c13] The method of claim 1, wherein the step of depositing a low-resistance material comprises depositing a low resistance material on the p-type transistor and the n-type transistor using evaporation, sputtering or chemical vapor deposition techniques.

[c14] An integrated circuit, comprising:
a p-type transistor having a polysilicon layer and a material with a low-resistance thereon;
an n-type transistor having a polysilicon layer and a material with a low-resistance thereon,
wherein a height of the polysilicon layer of the p-type

transistor is less than a height of a polysilicon layer of the n-type transistor.

[c15] The device of claim 14, wherein the height of the polysilicon of the p-type transistor is about 250Åto about 750 Å.

[c16] The device of claim 14, wherein the height of the polysilicon of the p-type transistor is about one-half the height of the polysilicon of the n-type transistor.

[c17] The device of claim 14, wherein the ratio of the height of the polysilicon of the p-type transistor to the ratio of the height of the polysilicon of the n-type transistor is about 1:2.

[c18] The device of claim 14, wherein the low-resistance material is one of Co, HF, Mo, Ni, Pd_2, Pt, Ta, Ti, W, and Zr, which when heated reacts with silicon to form a silicide.

[c19] The device of claim 14 wherein a height of the low resistance material on the p-type transistor is greater than a height of the low resistance material on the n-type transistor.

[c20] A method for manufacturing an integrated circuit comprising a plurality of semiconductor devices including an n-type transistor and a p-type transistor, the method

comprising:

forming a polysilicon layer on the n-type transistor and the p-type transistor, wherein the polysilicon layer on the p-type transistor has a shorter height than the polysilicon layer on the n-type transistor;

depositing a low-resistance material on the p-type transistor and the n-type transistor; and

heating the integrated circuit such that the deposited low-resistance material reacts with the polysilicon of the p-type transistor and the polysilicon of the n-type transistor, such that compressive mechanical stresses are formed along a longitudinal direction of a channel of the p-type transistor.